

Architecture Level Power Reduction Method for Configurable Processor Generation

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Outline

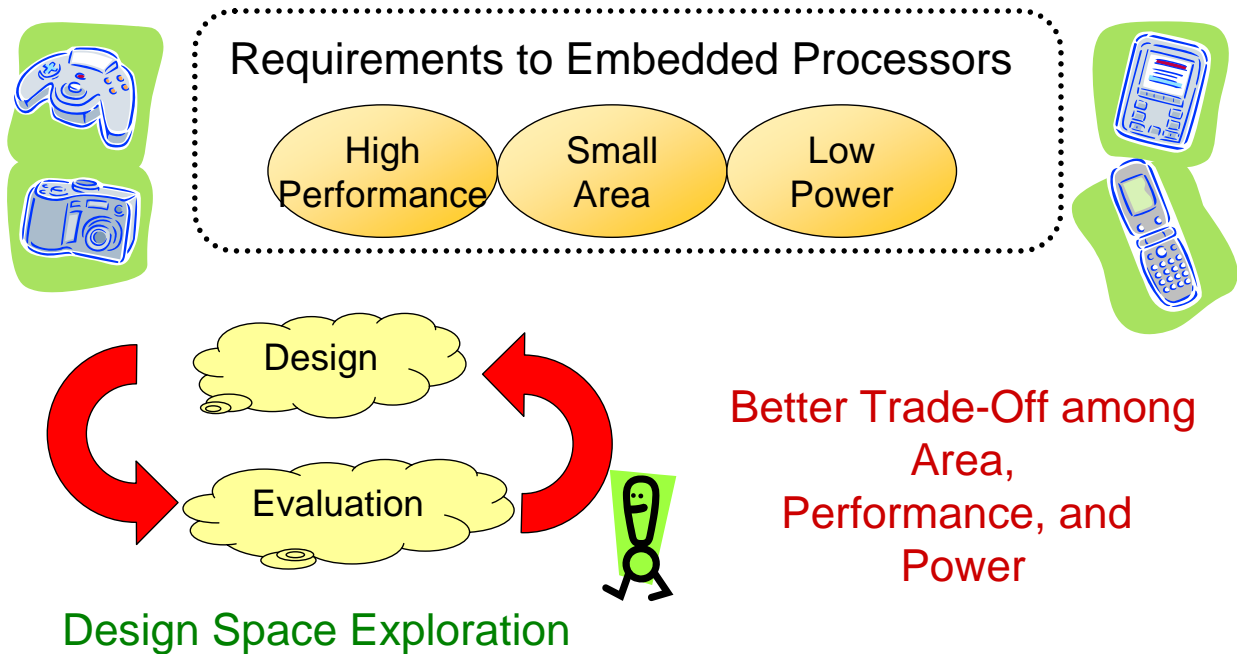
- Introduction
- Clock Gating
- VLIW Processor Generation Flow
- Extracting Non-Redundant Activation Conditions (NRAC)
- Experimental Results
- Conclusion

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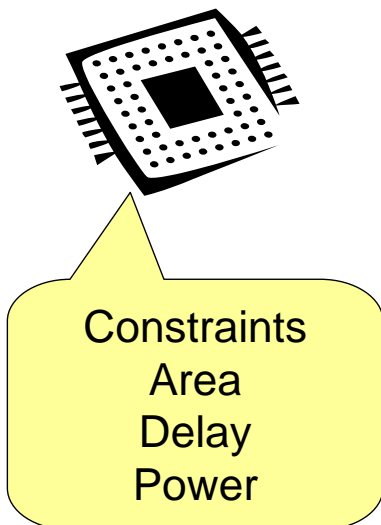
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Background



VLIW Processors

VLIW Processors



□ Advantage

- High Performance due to Instruction-set Level Parallelism (ILP)
- Less Power Consumption than Super Scalar Processor

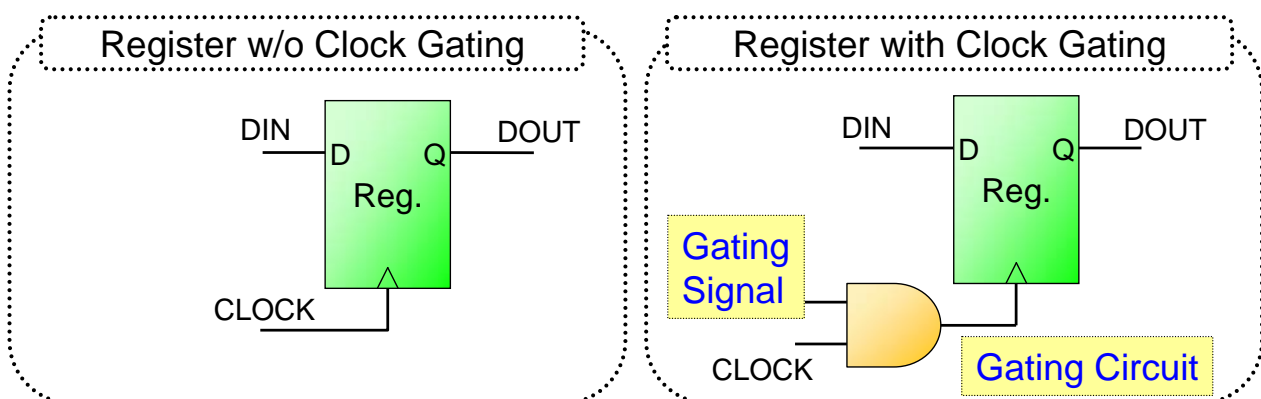
□ Issues to be Solved

- Better Design Space Exploration Methodology for Low Power VLIW Processors
- Better Power Reduction Method for Configurable VLIW Processors

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Clock Gating



- Clock Gating
 - Enables to Shut Off Clock Supplies According to Gating Signals
- Key Point
 - How to extract Non-Redundant Activation Condition

Related Work (1)

- Power Compiler, Synopsys Inc.
 - Clock gating insertion tool from RTL descriptions
 - Power Compiler does not modify gating signals
- Monteiro, J.C., et al.: “Implicit FSM Decomposition applied to Low-Power Design,” IEEE Trans. on VLSI Systems, Vol. 10, Issue 5, pp. 560-565, Oct. 2002.
 - Improves Gating Signals by Reforming FSM
 - Controller based on FSM is NOT Suitable for Pipeline Processors

Related Work (2)

- Babighian, P., et al.: “A Scalable Algorithm for RTL Insertion of Gated Clocks based on ODCs Computation,” IEEE Trans. on CAD of Integrated Circuits and Systems, Vol. 24, Issue 1, pp. 29-42, Jan. 2005
 - Improves Gating Signals by Calculating Observability Don't Care Conditions
 - Causes Enormous Amount of Area Overhead

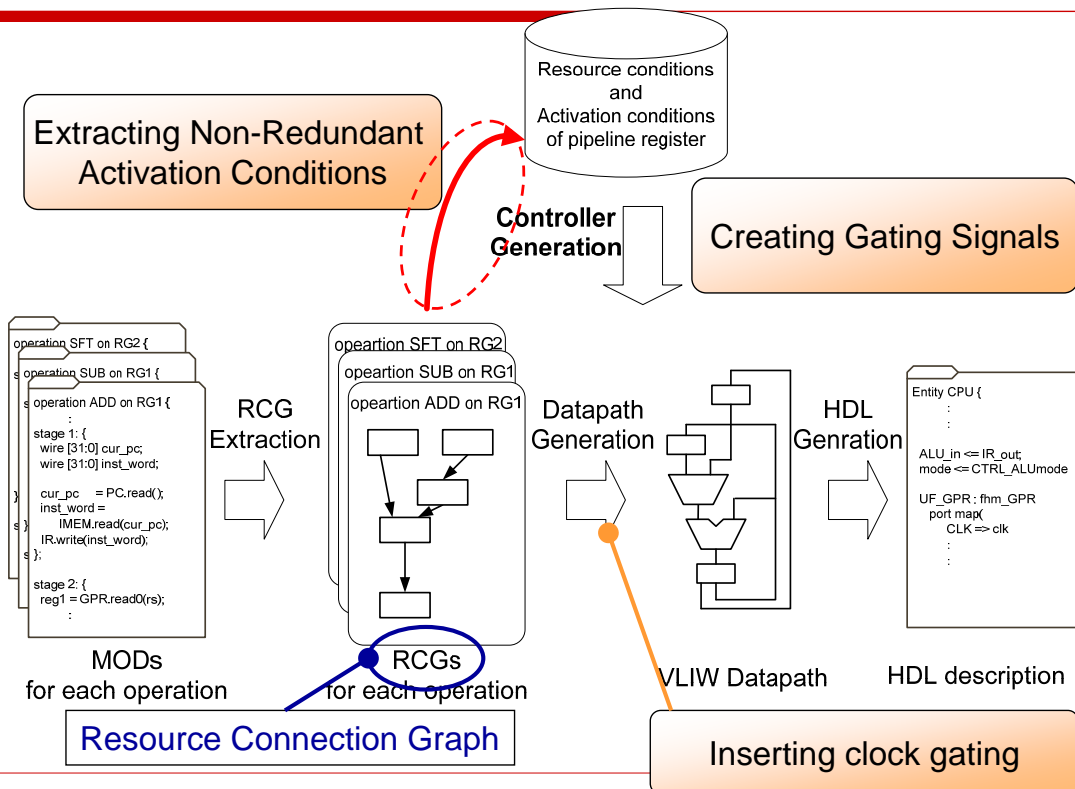
Contribution of Our Proposed Method

- Non-Redundant Activation Conditions (NRAC)
 - Conditions for Supplying Only Necessary Clocks to Pipeline Registers
 - Maximize Power Reduction Effect by Clock Gating
- Extracting NRAC from High Level Architecture Information (MOD: Micro-Operation Description)
 - Not Analyzing Generated Circuit
 - Extract NRAC during Processor Generation Process

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VLIW Processor Generation Flow



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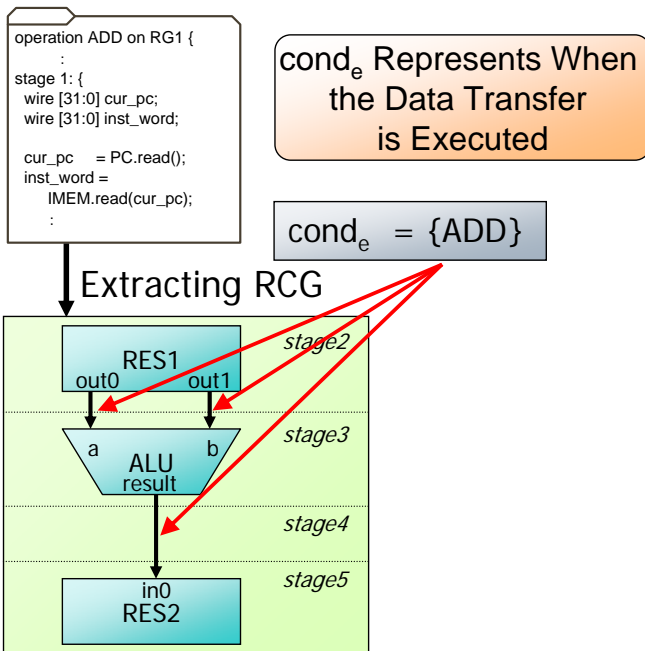
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NRAC Extraction

- ❑ RCG (Resource Connection Graph) Extraction
- ❑ Merging RCG
- ❑ Signal Conflict Resolution
- ❑ Pipelining

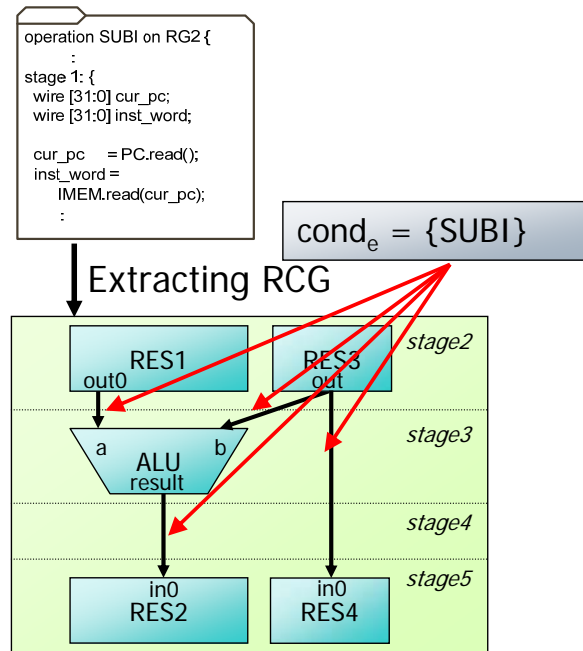
RCG Extraction

The MOD of ADD



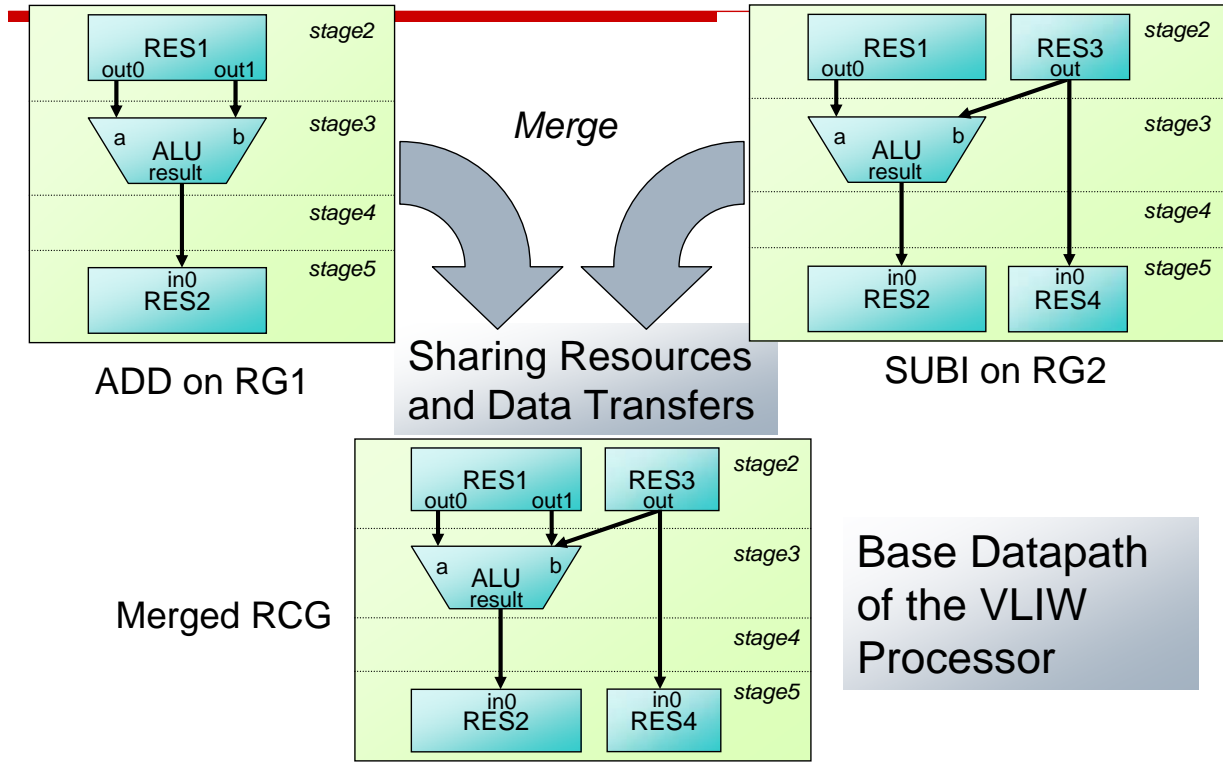
The RCG of ADD

The MOD of SUBI



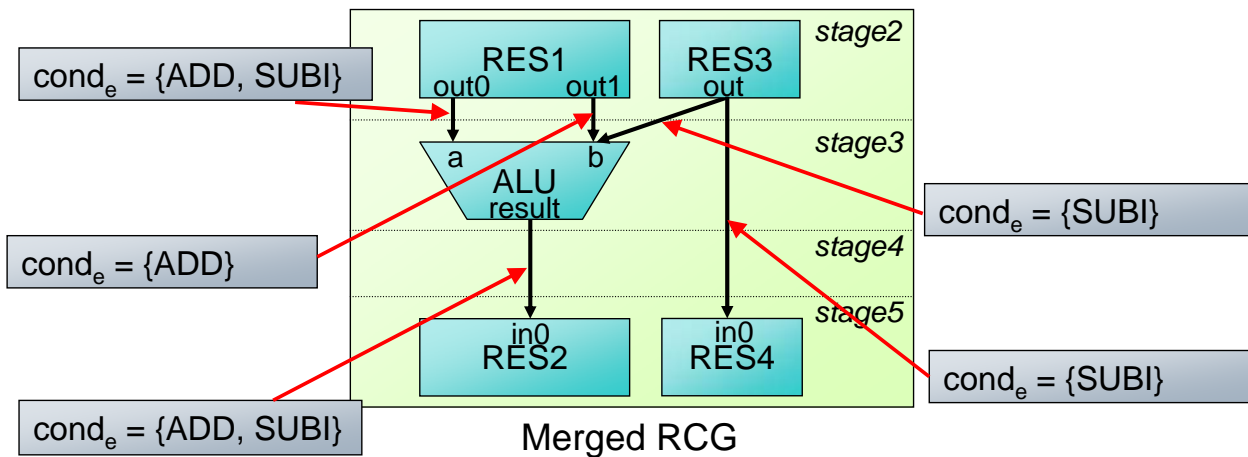
The RCG of SUBI

Merging RCG

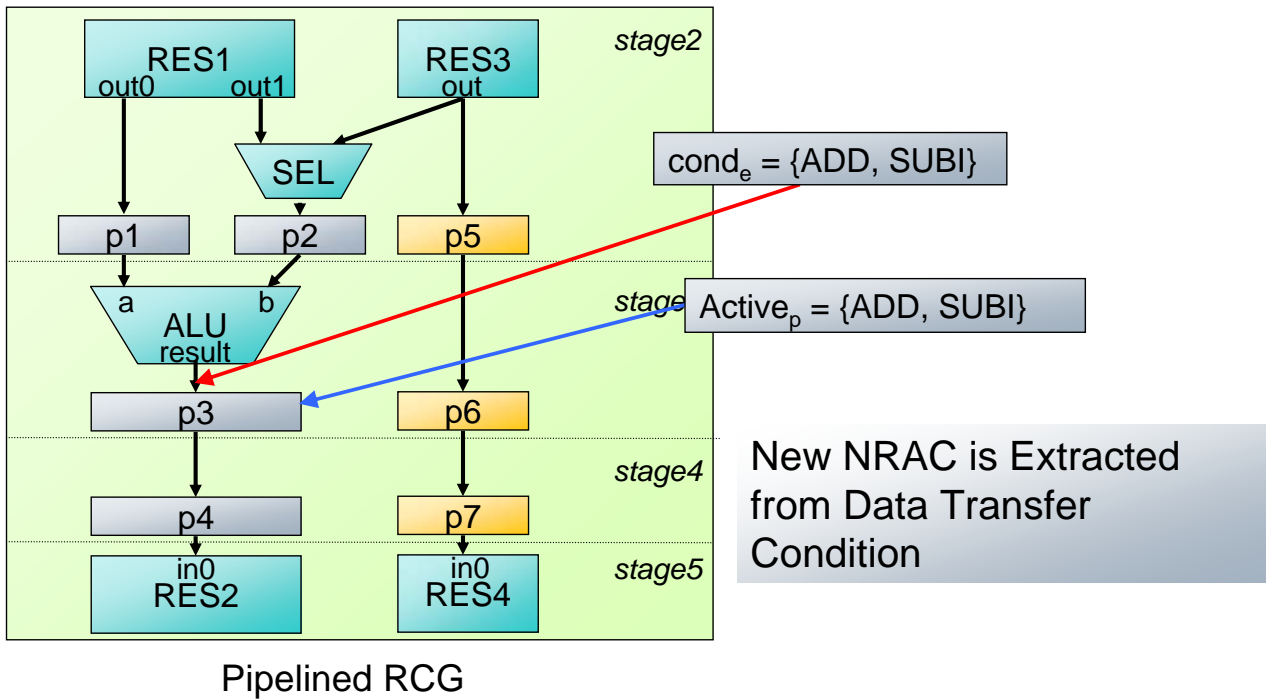


New Conditions of Merged Data Transfer

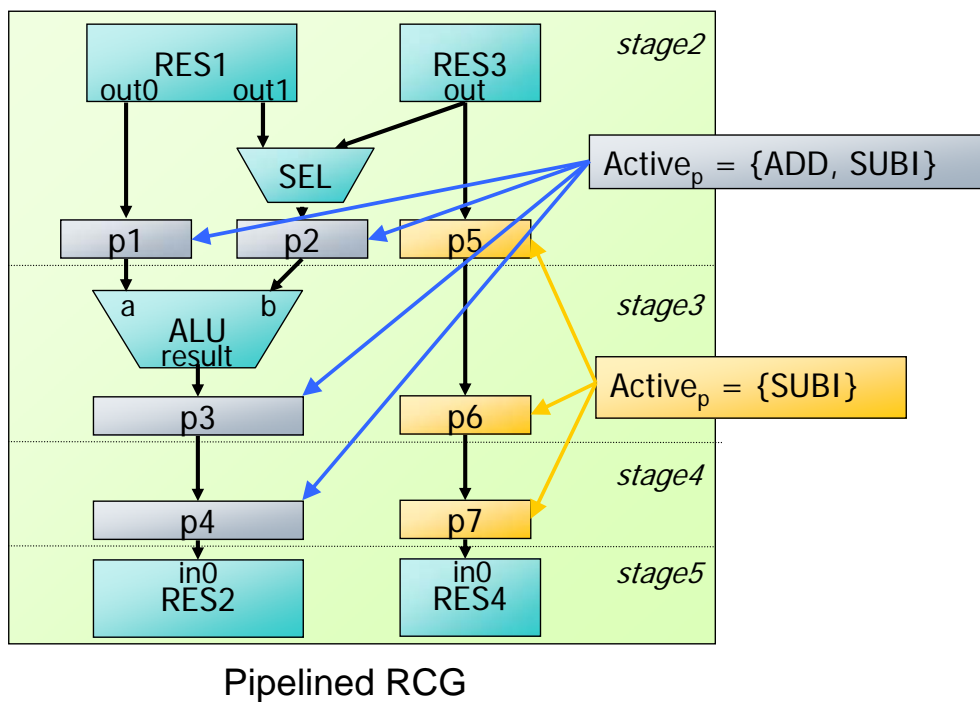
The Data Transfer Conditions are Unified



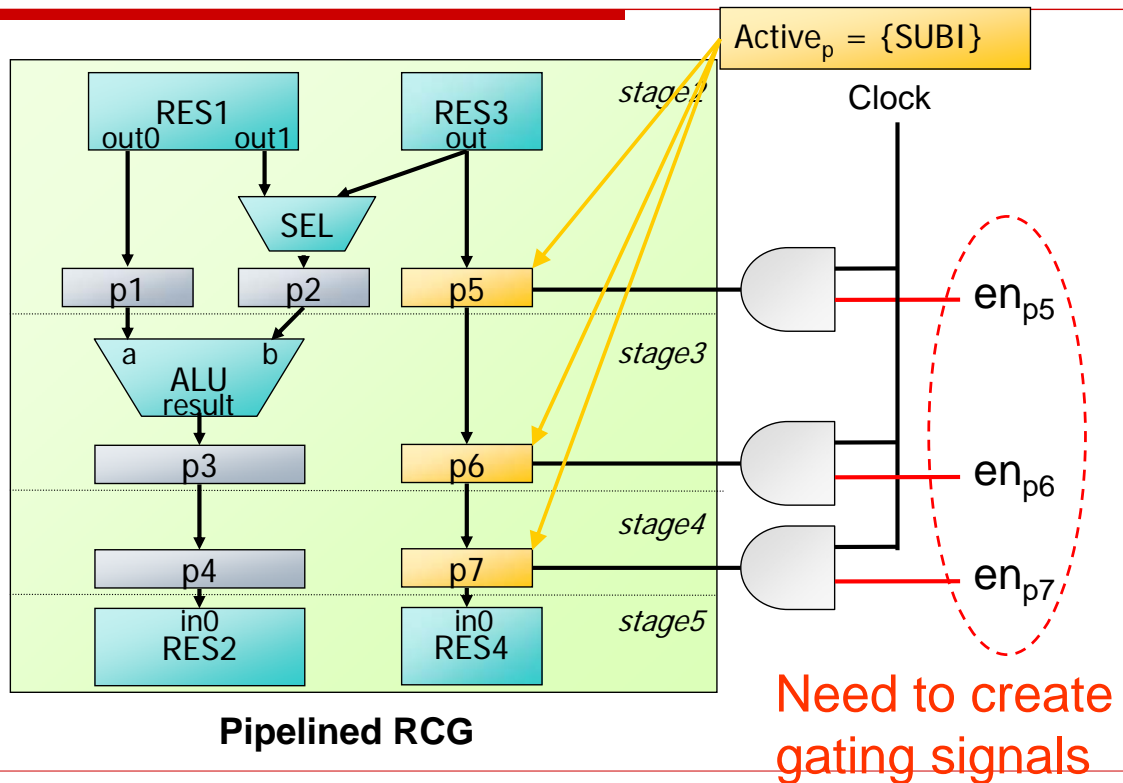
NRAC Extraction from Data Transfer Condition



NRAC for Pipeline Register Activation (1)



NRAC for Pipeline Register Activation (2)



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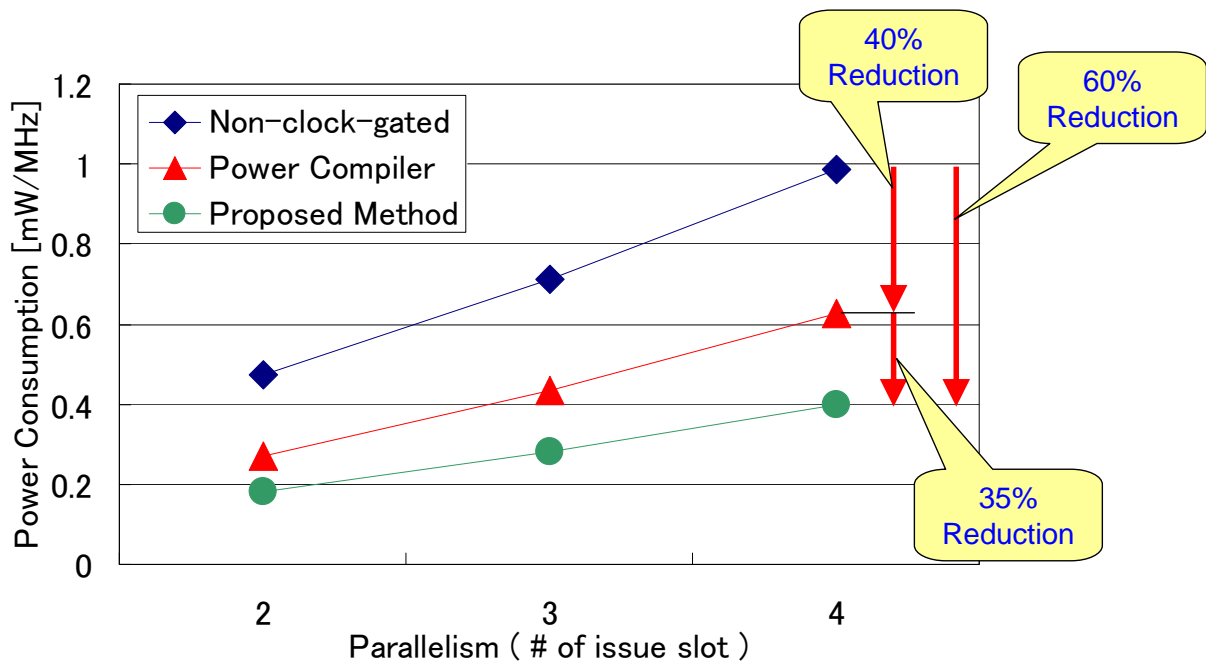
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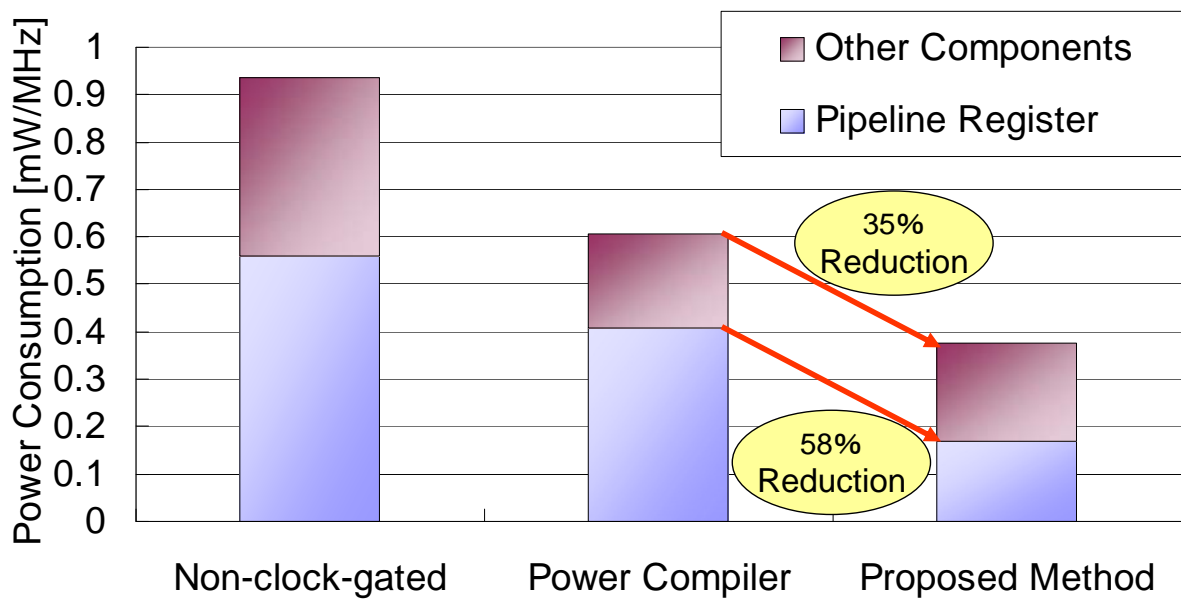
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Total Power Reduction



Total Power Reduction



■ VLIW Processor with 4 Issue Slots

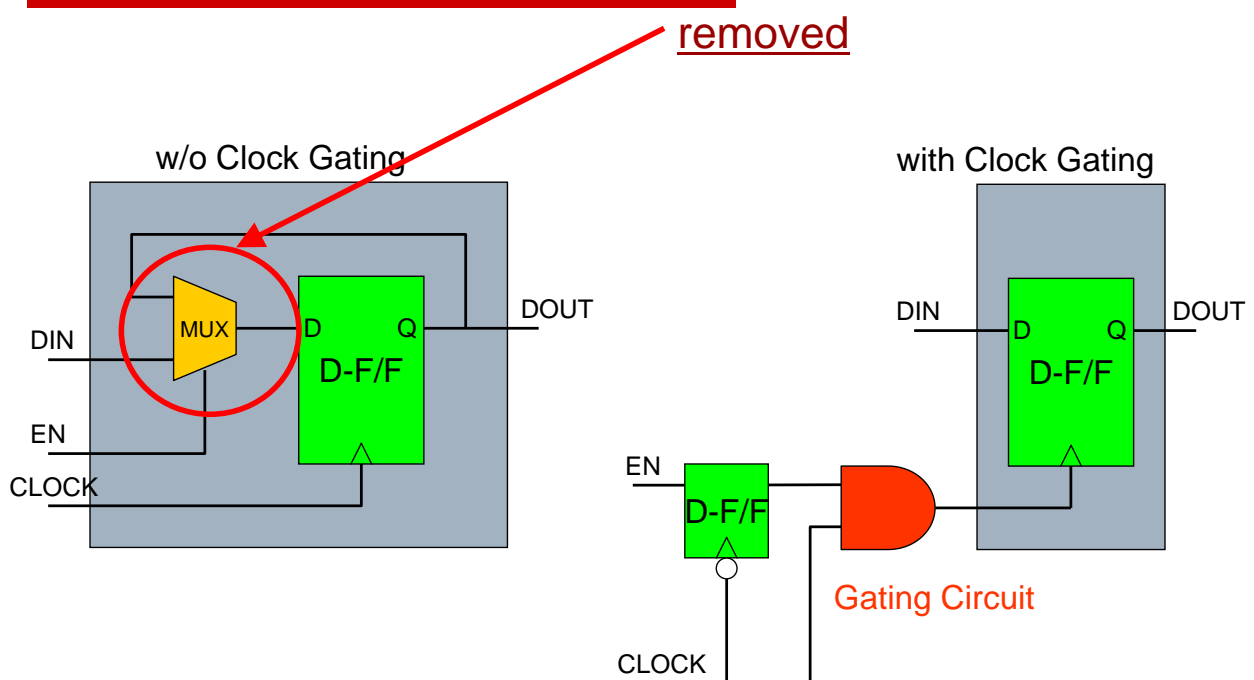
Area vs. the Number of Parallel Issue Slot

Processor	Parallel Issue #		
	2	3	4
Non-clock-gated	70,280	113,083	168,929
Power Compiler	63,589	101,890	152,517
Proposed Method	63,857	102,346	153,366
Overhead(gates)	269	456	848
Overhead(%)	0.42%	0.45%	0.56%

(Unit : Gates)

Area Overhead is Negligible

Area Reduction by Clock Gating



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Conclusion

- A Low Power VLIW Processor Generation Method has been Proposed
- Experimental Results Show
 - Efficient Power Reduction
 - ~60% Less Power than Non-Clock-Gating
 - ~35% Less Power than Power Compiler
 - Power Reduction of Pipeline Register is Dominant
 - ~70% Less Power than Non-Clock-Gating
 - ~60% Less Power than Power Compiler
 - Area Overhead is Negligible
 - 0.5% More Area than Power Compiler